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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/598,584	09/05/2006	Adrianus Josephus Bink	NL040237	7391

65913 7590 06/15/2009

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EXAMINER	
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ART UNIT	PAPER NUMBER
2183	

NOTIFICATION DATE	DELIVERY MODE
06/15/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/598,584	BINK ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 September 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-18 are pending.

2. The office acknowledges the following papers:

Patent Application filed on 9/5/2006.

Priority

3. The effective filing date for the subject matter defined in the pending claims in this application is 9/5/2006.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitations from claims 6-8 and 15-16 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d).

Specification

5. The disclosure is objected to because of the following informalities:

6. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. The Applicant’s cooperation is requested in correcting any errors of which the Applicant may become aware.

7. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is suggested: "Method for reducing current peak in an asynchronous processor".

8. Appropriate correction is required.

Claim Objections

9. Claim 1-18 are objected to because of the following informalities:

10. Claim 1 recites "the pipeline stages" at line 3 that should be changed to "the first and second pipeline stages" for proper antecedent basis.

11. Claim 1 recites "a latch" at line 3 that should be changed to "a first latch" so that proper antecedent basis in claims 4-5, 7, and 11 are established.

12. Claim 1 recites "the latch" at lines 5-6 and 8 that should be changed to "the first latch" for proper antecedent basis.

13. Claim 2 recites "the latch" at lines 2-3 and 5 that should be changed to "the first latch" for proper antecedent basis.

14. Claims 2-12 recite "An electronic circuit" at line 1 that should be changed to "The [[An]] electronic circuit" for proper antecedent basis.

15. Claim 4 recites "the current peaks" at line 4 that should be changed to "the current peak[[s]]" for proper antecedent basis.

16. Claim 4 recites "the latches" at lines 4-5 that should be changed to "the first and second latches" for proper antecedent basis.

17. Claim 6 recites "the latch" at line 2 that should be changed to "the one of the first and second latches [[latch]]" for proper antecedent basis.

18. Claim 13 recites "the stages" at line 3 that should be changed to "the first and second pipeline stages" for proper antecedent basis.

19. Claim 13 recites "a latch" at line 3 that should be changed to "a first latch" so that proper antecedent basis in claims 15-17 are established.

20. Claim 13 recites "the latch" at lines 4-7 that should be changed to "the first latch" for proper antecedent basis.

21. Claims 11 and 15-17 recite "second latch" at lines 2-3 that should be changed to "the second latch" for proper antecedent basis.

22. Claim 14-18 recites "A method" at line 1 that should be changed to "The [[A]] method" for proper antecedent basis.

Double Patenting

23. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to

be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

24. Claims 1-2 and 13 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-2 of copending Application No. 10/598,583. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1-2 and 13 of the instant application are anticipated by claims 1-2 of the copending application. Claims 1-2 and 13 of the instant application therefore are not patently distinct from the earlier patent claim and as such is unpatentable for obvious-type double patenting. Cf., Titanium Metals Corp. v. Banner, 778 F.2d 775, 227 USPQ 773 (Fed. Cir. 1985) (holding that an earlier species disclosure in the prior art defeats any generic claim). This court's predecessor has held that, without a terminal disclaimer, the species claims preclude issuance of the generic application. In re Van Ornum, 686 F.2d 937, 944, 214 USPQ 761, 767 (CCPA 1982); Schneller 397 F.2d at 354. Accordingly, absent a terminal disclaimer, claims 12 and 13 were properly rejected under the doctrine of obviousness-type double patenting." (In re Goodman (CA FC) 29 USPQ2d 2010 (12/3/1993).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Instant Application	Application # 10/598,583
1. An electronic circuit comprising:	1. An electronic circuit adapted to process a plurality of types of instruction, the electronic circuit comprising:

First and second pipeline stages; and	First and second pipeline stages, each pipeline stage generating pipeline data;
A latch positioned between the pipeline stages;	A latch positioned between the pipeline stages; and
Wherein the electronic circuit is adapted to operation in a normal mode in which the latch is opened and closed in response to an enable signal, and	Wherein the electronic circuit is controlled by a control signal based on a latency period of each respective instruction of said plurality of types of instruction, said electronic circuit being controlled to operate in a normal mode when processing a first type of instruction in which the latch is opened and closed in response to an enable signal, and
A reduced mode in which the latch is held open to reduce a current peak associated with the opening and closing of the latch.	A reduced mode including a truncated passage when processing a second type of instruction in which the enable signal is overridden by the control signal so that the latch is held open for the generated pipeline data to propagate, independent of the enable signal, through the latch; and
	Wherein the first type of instruction requires processing by the first and second pipeline stages and the second type of instruction requires processing by the second pipeline stage.

Independent Claim 13 is similar to claim 1 and is rejected for the same reasons.

25. Claims 1-18 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-3 of U.S. Patent No. 7,423,449 in view of Hennessy et al. (“Computer Organization and Design: The Hardware/Software Interface”), in view of Colwell et al. (U.S. 5,604,878).

Instant Application	U.S. 7,423,449
1. An electronic circuit comprising:	1. An electronic circuit comprising:
First and second pipeline stages; and	First and second combinational logic blocks; and
A latch positioned between the pipeline stages;	A latch positioned between the combinational logic blocks;
Wherein the electronic circuit is adapted to	Wherein the electronic circuit is adapted to

operation in a normal mode in which the latch is opened and closed in response to an enable signal, and	operation in a normal mode in which the latch is opened and closed in response to an enable signal, and
A reduced mode in which the latch is held open to reduce a current peak associated with the opening and closing of the latch.	
	A test mode in which the latch is held open, such that the latch is transparent.

Independent Claim 13 is similar to claim 1 and is rejected for the same reasons. The limitations not shown by the claims in U.S. 7,423,449 are read upon as specified by the rejection below.

26. Claims 3-12 and 14-18 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-2 of copending Application No. 10/598,583 in view of Hennessy et al. ("Computer Organization and Design: The Hardware/Software Interface"), in view of Colwell et al. (U.S. 5,604,878). This is a provisional obviousness-type double patenting rejection. The limitations not shown by application No. 10/598,583 are read upon as specified by the rejection below.

Claim Rejections - 35 USC § 112

27. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

28. Claims 8, 10-12, and 18 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 10 recites “the latch control circuits.” Claim 10 is dependent upon claim 9, which states a second latch control circuit. Claim 2 recites a latch control circuit for the first latch, but this claim isn’t included in claim 10 because of different dependencies. Thus, claim 10 only contains a single latch control circuit. For examination purposes, the limitation will be interpreted as “the second latch control circuit.”

Claim 12 recites “each latch control circuit.” Claim 12 is dependent upon claim 9, which states a second latch control circuit. Claim 2 recites a latch control circuit for the first latch, but this claim isn’t included in claim 10 because of different dependencies. Thus, claim 12 only contains a single latch control circuit. For examination purposes, the limitation will be interpreted as “the second latch control circuit.”

29. Claims 8 and 18 recites the limitation "the length of time" in lines 1-2 of the claims. There is insufficient antecedent basis for this limitation in the claims. For examination purposes, no antecedent basis is established.

30. Claim 10 recites the limitation "the mode of operation" in lines 2-3 of the claim. There is insufficient antecedent basis for this limitation in the claim.

31. Claims 11 are rejected due to their dependency.

Claim Rejections - 35 USC § 103

32. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

33. Claims 1-18 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hennessy et al. ("Computer Organization and Design: The Hardware/Software Interface"), in view of Colwell et al. (U.S. 5,604,878).

34. As per claim 1:

Hennessy disclosed an electronic circuit comprising:

first and second pipeline stages (Hennessy: Figure 6.25, pipeline stages MEM and WB); and

a latch positioned between the pipeline stages (Hennessy: Figure 6.25, MEM/WB pipeline register)(It's obvious to one of ordinary skill in the art that the pipeline register can be implemented as a latch.);

wherein the electronic circuit is adapted to operate in a normal mode in which the latch is opened and closed in response to an enable signal (Hennessy: Figures 6.32 and 6.33, load instruction)(The MEM/WB pipeline register is opened and closed by the inherent clock signal of the processor not shown, which is the enable signal.).

Hennessy failed to teach a reduced mode in which the latch is held open to reduce a current peak associated with the opening and closing of the latch.

However, Colwell disclosed a reduced mode in which the latch is held open to reduce a current peak associated with the opening and closing of the latch (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(Hennessy: Figure 6.33, sub instruction)(The combination uses elements 61-62 to bypass the MEM/WB pipeline register by keeping the pipeline register open when a

writeback contention will be avoided. The control signal is the signal from element 62 that allows for two pipeline stages to affectively become a single stage.).

The advantage of bypassing an extra pipeline stage that isn't needed for instructions is that these instructions will be allowed to retire earlier and result in increased performance when there is no writeback contention (Colwell: Column 2 lines 65-67 continued to column 3 lines 1-9). One of ordinary skill in the art would have been motivated to modify Hennessy to perform the pipeline stage bypassing of Colwell for the advantage above. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the pipeline stage bypassing of Colwell into the processor of Hennessy for the advantage of increasing performance of the processor of Hennessy.

35. As per claim 2:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim 1, further comprising a latch control circuit connected to the latch, the latch control circuit being adapted to control the latch with the enable signal when the electronic circuit is in the normal mode (Hennessy: Figures 6.32 and 6.33, load instruction)(The MEM/WB pipeline register is opened and closed by the inherent clock signal of the processor not shown, which is the enable signal.), and to hold the latch open when the electronic circuit is in the reduced mode (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(Hennessy: Figure 6.33, sub instruction)(The combination uses elements 61-62 to bypass the MEM/WB pipeline register when a

writeback contention will be avoided, which results in holding open the MEM/WB pipeline register.).

36. As per claim 3:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim 1, the electronic circuit further comprising a third pipeline stage and a second latch, the second latch positioned between the second and third pipeline stages (Hennessy: Figure 6.25, pipeline stages EX and MEM)(The third pipeline stage can be considered the execution stage, where the latch is the EX and MEM pipeline stages.).

37. As per claim 4:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim 3, wherein, when the electronic circuit is operating in the reduced mode, both of the first and second latches are held open to reduce the current peaks associated with the opening and closing of the latches (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(Hennessy: Figure 6.33, sub instruction)(The advantage of longer pipelines is that increased performance can be achieved by executing more instructions in parallel. Official notice is given that pipelines can be of greater length than five stages. Thus, it's obvious to one of ordinary skill in the art that pipelines can be longer than five stages. With a longer pipeline, the data memory and writeback stages can be multiple stages, which requires multiple latches to be opened to execute instructions that don't use the data memory stage.).

38. As per claim 5:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim 3, wherein, when the electronic circuit is operating in the reduced mode, one of the first and second latches is held open to reduce the current peak associated with the opening and closing of that latch (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(Hennessy: Figure 6.33, sub instruction)(The combination uses elements 61-62 to bypass the MEM/WB pipeline register by keeping the pipeline register open when a writeback contention will be avoided. The control signal is the signal from element 62 that allows for two pipeline stages to affectively become a single stage.).

39. As per claim 6:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim 5, wherein the latch held open changes over time (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(Hennessy: Figure 6.33, sub instruction)(The combination uses elements 61-62 to bypass the MEM/WB pipeline register by keeping the pipeline register open when a writeback contention will be avoided. Both latches are held open in normal mode when clocked, and a single latch is held open in reduced mode to allow an ALU type instruction to bypass the MEM stage. Thus, the latches held open changes during executing a program.).

40. As per claim 7:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim 6, wherein the first and second latches are held open for different lengths of time (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-

3)(Hennessy: Figure 6.33, sub instruction)(The first latch is the latch between the MEM and WB stages and the second latch is the latch between the EX and MEM stages. The combination uses elements 61-62 to bypass the MEM/WB pipeline register by keeping the pipeline register open when a writeback contention will be avoided. Thus, the first latch can be held open for a different amount of time than the second latch.).

41. As per claim 8:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim 1, wherein the length of time that the electronic circuit operates in the reduced mode varies (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(Hennessy: Figure 6.33, sub instruction)(The combination uses elements 61-62 to bypass the MEM/WB pipeline register by keeping the pipeline register open when a writeback contention will be avoided. The control signal is the signal from element 62 that allows for two pipeline stages to affectively become a single stage. The latch can operate in reduced mode for different lengths of time dependent upon the type of instructions sent into the pipeline.).

42. As per claim 9:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim 3, further comprising a second latch control circuit connected to the second latch (Hennessy: Figures 6.32 and 6.33, load instruction)(The EX/MEM pipeline register is opened and closed by the inherent clock signal of the processor not shown, which controls the second latch.).

43. As per claim 10:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim 9, wherein the latch control circuits receive a signal indicating the mode of operation of the electronic circuit (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(The control logic generates a signal that determines the mode of the processor when Hennessy is acting as a 4 or 5 stage pipeline.).

44. As per claim 11:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim 10, wherein the signal indicates whether the first latch, second latch or both latches are to be held open when the electronic circuit is operating in the reduced mode (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(Hennessy: Figure 6.33, sub instruction)(The combination uses elements 61-62 to bypass the MEM/WB pipeline register by keeping the pipeline register open when a writeback contention will be avoided. The control signal is the signal from element 62 that allows for two pipeline stages to affectively become a single stage. The first latch is selected to be held open in the reduced mode.).

45. As per claim 12:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim 9, wherein each latch control circuit receives a respective control signal, indicating whether its respective latch is to be held open when the electronic circuit is operating in the reduced mode (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(Hennessy: Figure 6.33, sub instruction)(The advantage of longer pipelines is that increased performance can be achieved by executing more instructions

in parallel. Official notice is given that pipelines can be of greater length than five stages. Thus, it's obvious to one of ordinary skill in the art that pipelines can be longer than five stages. With a longer pipeline, the data memory and writeback stages can be multiple stages, which requires multiple latches to be opened to execute instructions that don't use the data memory stage. Each latch inherently receives control signals to tell if the latch is to be held open or closed at a given period of time.).

46. As per claim 13:

Claim 13 essentially recites the same limitations of claim 1. Therefore, claim 13 is rejected for the same reasons as claim 1.

47. As per claim 14:

The additional limitation(s) of claim 14 basically recite the additional limitation(s) of claim 4. Therefore, claim 14 is rejected for the same reason(s) as claim 4.

48. As per claim 15:

Hennessy and Colwell disclosed an method as claimed in claim 14, wherein the first latch and second latch are held open at different times when the electronic circuit is operating in the reduced mode (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(Hennessy: Figure 6.33, sub instruction)(The first latch is the MEM/WB pipeline register and the second latch is the EX/MEM pipeline register. The combination uses elements 61-62 to bypass the MEM/WB pipeline register by keeping the pipeline register open when a writeback contention will be avoided. Thus, when the processor operates in a reduced mode, the first latch is open during execution while the second latch is closed.).

49. As per claim 16:

The additional limitation(s) of claim 16 basically recite the additional limitation(s) of claim 7. Therefore, claim 16 is rejected for the same reason(s) as claim 7.

50. As per claim 17:

The additional limitation(s) of claim 17 basically recite the additional limitation(s) of claim 4. Therefore, claim 17 is rejected for the same reason(s) as claim 4.

51. As per claim 18:

The additional limitation(s) of claim 18 basically recite the additional limitation(s) of claim 8. Therefore, claim 18 is rejected for the same reason(s) as claim 8.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Jacobson (U.S. 7,076,682), taught holding asynchronous pipeline stage's latches open when not used.

Lin et al. (U.S. 7,406,588), taught bypassing pipeline registers when data isn't valid.

Bose et al. (U.S. 7,076,681), taught reducing power consumption by holding pipeline registers closed on stalls.

Cook et al. (U.S. 6,848,060), taught an asynchronous to synchronous interface.

Tiwari et al. (U.S. 6,609,209), taught clock gating pipeline registers to reduce power consumption.

Jacobson et al. (U.S. 7,065,665), taught interlocked synchronous pipeline clock gating.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Jacob Petranek/
Examiner, Art Unit 2183